WHAT IS CLAIMED IS:

1. A field emission display, comprising:

a first substrate;

at least one gate electrode formed in a predetermined pattern on the first substrate;

a plurality of cathode electrodes formed on the first substrate in a predetermined pattern;

at least one first insulation layer formed between the at least one gate electrode and the plurality of cathode electrodes;

at least one emitter mounted within an opening of the cathode electrode;

at least one second insulation layer being formed on the cathode electrode;

at least one focusing electrode formed on the second insulation layer;

a second substrate provided opposing the first substrate with a predetermined gap therebetween, the first and second substrates forming a vacuum assembly when interconnected;

at least one anode electrode formed on the second substrate opposing the first substrate; and

phosphor layer formed on the at least one anode electrode in a pattern corresponding to positions of the emitter.

2. The field emission display of claim 1, wherein the cathode electrodes and the gate electrodes are crossed in a striped pattern.

3. The field emission display of claim 1, wherein the cathode electrodes and the anode electrodes are crossed in a striped pattern.

4. The field emission display of claim 1, wherein the second insulation layer has a channel formed corresponding to the emitter, the second insulation layer being formed on the cathode electrode such that the emitter is positioned within the channel.

5. The field emission display of claim 1, wherein the emitter is formed as longitudinal single structure with long ends in a direction along which the gate electrode is patterned.

6. The field emission display of claim 1, wherein the channel is formed by a stepped portion of the second insulation layer.

7. The field emission display of claim 6, wherein the second insulation layer includes first sub-insulation layer having an opening formed to substantially identical dimensions as the opening of the cathode electrode when viewing the field emission display in a first direction normal to an outer surface of the second substrate, and second sub-insulation layer having an opening that is larger than the opening of the first sub-insulation layers when viewed in the first direction,

wherein the channel is formed by the opening of the first sub-insulation layer and the opening of the second sub-insulation layer.

8. The field emission display of claim 7, wherein the channel is formed by sequentially depositing the first and second sub-insulation layer having different sizes to thereby form the stepped portion of the second insulation layer.

9. The field emission display of claim 7, wherein the focusing electrode

is formed by coating a conductive material on upper surfaces of the first sub-insulation layer and on upper surfaces and side walls of the second sub-insulation layer.

10. The field emission display of claim 1, wherein the second insulation layer is opaque.

11. The field emission display of claim 1, wherein the emitter includesi carbon nanotubes.

12. The field emission display of claim 1, wherein the emitter is divided into a plurality of sections for each pixel.

13. A field emission display, comprising:

a first substrate;

a plurality of gate electrodes formed in a predetermined pattern on the first substrate;

a plurality of cathode electrodes formed on the first substrate in a predetermined pattern, the cathode electrodes forming intersection regions with the gate electrodes corresponding to pixel regions;

at least one first insulation layer between the at least one gate electrode and the plurality of cathode electrodes;

an emitter mounted within openings of the cathode electrodes formed in the intersection regions;

a second insulation layer having a plurality of channels formed corresponding to the emitters, the second insulation layer being formed on the cathode electrodes such that the emitters are positioned within the channels;

focusing electrodes formed on the second insulation layer;

a second substrate provided opposing the first substrate with a predetermined gap wherebetween, the first and second substrate forming a vacuum assembly when interconnected;

an anode electrode formed on at least one side of the second substrate opposing the first substrate; and

phosphor layers formed on at least one side of the anode electrode in a pattern corresponding to positions of the emitters.

14. The field emission display of claim 13, wherein the emitters are formed as longitudinal single structures with long ends in a direction along which the gate electrodes are patterned.

15. The field emission display of claim 13, wherein the channels are formed by a stepped portion of the second insulation layer.

16. The field emission display of claim 15, wherein the second insulation layer includes first sub-insulation layers having openings formed to substantially identical dimensions as the openings of the cathode electrodes when viewing the field emission display in a first direction normal to an outer surface of the second substrate, and second sub-insulation layers having openings that are larger than the openings of the first sub-insulation layers when viewed in the first direction.

17. The field emission display of claim 16, wherein the channels are formed by sequentially depositing the first and second sub-insulation layers having different sizes to thereby form the stepped portion of the second insulation layer.

18. The field emission display of claim 16, wherein the focusing

electrodes are formed by coating a conductive material on upper surfaces of the first sub-insulation layers and on upper surfaces and side walls of the second sub-insulation layers.

19. The field emission display of claim 13, wherein the second insulation layer is opaque.

20. The field emission display of claim 13, wherein the emitters are carbon nanotubes.

21. A field emission display, comprising:

a first substrate;

at least one gate electrode formed in a predetermined gate electrode pattern on the first substrate;

a plurality of cathode electrodes formed on the first substrate in a predetermined pattern;

at least one first insulation layer formed between the at least one gate electrode and the plurality of cathode electrodes;

emitters electrically contacting the cathode electrodes;

a second substrate opposing the first substrate with a predetermined gap therebetween, the first substrate and the second substrate forming a vacuum container;

at least one anode electrode formed in a predetermined anode electrode pattern on a surface of the second substrate opposing the first substrate; and

phosphor layers formed in a predetermined phosphor layer pattern on the anode electrode;

wherein portions of the cathode electrodes are removed to form emitter-receiving sections, one of the emitters being provided in each of the emitter-receiving sections electrically contacting the cathode electrodes;

wherein a pixel region is formed between an emitter and a respective phosphor layer of the predetermined phosphor layer pattern at each intersection of:

a cathode electrode and a gate electrode when the anode electrode is a common anode electrode, or

a cathode electrode and an anode electrode when the gate electrode is a common gate electrode; and

wherein predetermined voltages are applied to the at least one anode electrode, cathode electrodes and the at least one gate electrode generating an electric field between respective gate electrodes and the emitters such that electrons emitted from emitters are induced toward and strike the phosphor layer in a corresponding pixel region to realize predetermined images.

22. The field emission display of claim 21, wherein the at least one gate electrode formed in a predetermined gate electrode pattern is a plurality of gate electrodes formed in a striped pattern and the at least one anode electrode formed in a predetermined anode electrode pattern is one anode electrode functioning as the common electrode.

23. The field emission display of claim 21, wherein the at least one anode electrode formed in a predetermined anode electrode pattern is a plurality of anode electrodes formed in a striped pattern and the at least one gate electrode formed in a predetermined gate electrode pattern is one gate

electrode functioning as the common electrode.